V. REMARKS

Claims 1-4 are rejected under 35 USC 102 (e) as being anticipated by Akiyama et al. (U.S. Patent Application Publication No. 2003/0020096). The rejection is respectfully traversed.

Akiyama discloses method of producing a bonded SOI wafer that includes a plurality of steps. One step is bonding a bond wafer and a base wafer via an oxide film and then reducing thickness of the bond wafer. A silicon single crystal ingot is grown according to Czochralski method and the single crystal ingot is then sliced to produce a silicon single crystal wafer. The silicon single crystal wafer is subjected to heat treatment in a non-oxidizing atmosphere at a temperature of 1100°C. to 1300°C. for one minute or more and continuously to a heat treatment in an oxidizing atmosphere at a temperature of 700°C. to 1300°C. for one minute or more without cooling the wafer to a temperature less than 700°C. to provide a silicon single crystal wafer. A silicon oxide film is formed on the surface. Thereafter, hydrogen ions and rare gas ions are implanted into the surface via a silicon oxide film of the wafer to form an ion implanted layer. The resultant wafer is used as the bond wafer, which is then brought into close contact with the base wafer via the silicon oxide film of the bond wafer, followed by delamination at the ion implanted layer by heat treatment.

Claim 1, as amended, is directed to a method for manufacturing an SOI wafer comprising the steps of:

providing two starting wafers with each starting wafer having at least one line-defect-free surface;

forming an insulating layer on the line-defect-free surface on at least one wafer of two starting wafers; and

adhering the one wafer to the other wafer without an adhesive with the line-defect-free surfaces facing each other.

It is respectfully submitted that the rejection is improper because the applied art fails to teach each and every element of claim 1 as amended. Specifically, it is respectfully submitted that the applied art fails to teach the steps of (1) providing two starting wafers with each starting wafer having at least one line-defect-free surface and (2) adhering the one wafer to the other wafer without an adhesive with the line-defect-free surfaces facing each other. Thus, it is respectfully submitted that claim 1 is allowable over the applied art.

Claim 2, as amended, is directed to a method for manufacturing an SOI wafer comprising the steps of:

forming an insulating layer on at least one wafer of the two starting wafers; and

adhering the one wafer to the other wafer without an adhesive.

Claim 2 recites the starting wafer is subjected to high temperature heat treatment in advance and the high temperature heat treatment is carried out at a high temperature of 1100°C or higher for at least one hour.

It is respectfully submitted that the rejection is improper because the applied art fails to teach each and every element of claim 2 as amended. Specifically, it is respectfully submitted that the applied art fails to teach that the starting wafer is subjected to high temperature heat treatment in advance and the high temperature heat treatment is carried out at a high temperature of 1100°C or higher for at least one hour . Thus, it is respectfully submitted that claim 2 is allowable over the applied art.

Claim 4 depends from claim 1 and includes all of the features of claim 1. Thus, it is respectfully submitted that the dependent claim is allowable at least for the reason claim 1 is allowable as well as for the features it recites.

Claim 3 is canceled and, as a result, the rejection as applied thereto is now moot.

Withdrawal of the rejection is respectfully requested.

Claims 5 and 6 are rejected under 35 USC 103 (a) as being unpatentable over Akiyama in view of Iwabuchi (U.S. Patent Application Publication No. 2002/0155630). The rejection is respectfully traversed.

Iwabuchi teaches methods of inspecting and manufacturing silicon wafer, method of manufacturing semiconductor device and silicon wafer. This invention provides a method for inspecting a silicon wafer making it possible to identify and efficiently detect a new defect affecting a device fabricating process, a method for manufacturing a silicon wafer enabling manufacture of wafers not having the defect, a method for fabricating a semiconductor device using the silicon wafer not having this defect and the silicon wafer not having the defect. When a silicon wafer is inspected, inspection is made for a defect having the entire defect size of 0.5 μm or more in which micro-defects gather in a colony state.

Claims 5 and 6 depend from claim 1 and includes all of the features of claim of claim 1. Thus, it is respectfully submitted that that the dependent claims are allowable at least for the reason claim 1 is allowable as well as for the features they recite.

Withdrawal of the rejection is respectfully requested.

Further, Applicants assert that there are also reasons other than those set forth above why the pending claims are patentable. Applicants hereby reserve the right to submit those other reasons and to argue for the patentability of claims not explicitly addressed herein in future papers.

In view of the foregoing, reconsideration of the application and allowance of the pending claims are respectfully requested. Should the Examiner believe

anything further is desirable in order to place the application in even better condition for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

Should additional fees be necessary in connection with the filing of this paper or if a Petition for Extension of Time is required for timely acceptance of the same, the Commissioner is hereby authorized to charge Deposit Account No. 18-0013 for any such fees and Applicant(s) hereby petition for such extension of time.

Respectfully submitted,

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Enclosure(s): Amendment Transmittal

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